## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A circuit comprising:

cache memory structure comprising multiple banks;

a plurality of access ports communicatively coupled to said cache memory structure;

circuitry operable to determine a bank conflict for pending access requests for said cache memory structure, wherein said circuitry is operable to determine said bank conflict using bits of virtual addresses to be accessed by said pending access requests, and wherein said bits of virtual addresses include bits that correspond to bits of physical addresses to be accessed by said pending access requests; and

circuitry operable to issue at least one access request to said cache memory structure out of the order in which it was requested, responsive to determination of said bank conflict.

2. (Original) The circuit of claim 1 wherein said bank conflict comprises a bank conflict between at least two access requests.

3. (Original) The circuit of claim 1 further comprising:

pending request queue to which said pending access requests for said cache memory structure are stored, wherein said bank conflict is determined for at least one pending access request upon entry of said at least one pending access request into said pending request queue.

4. (Original) The circuit of claim 3 wherein said bank conflict comprises a bank conflict between at least one pending access request and least one issued access request.

5. (Original) The circuit of claim 1 wherein said circuitry operable to issue at least one access request is further operable to issue said at least one access request according to a predefined pipeline, said predefined pipeline having a plurality of stages with one stage for performing a first type of access and a different stage for performing a second type of access.

6. (Original) The circuit of claim 5 wherein said bank conflict comprises a bank conflict between at least one access request of said first type with at least one access request of said second type.

7. (Original) The circuit of claim 5 wherein said first type of access request comprises a request for a data store operation to a particular bank of said cache memory structure, and wherein said second type of access request comprises a request for a data read operation to said particular bank of said cache memory structure.

8. (Original) The circuit of claim 5 wherein said pipeline comprises:

a stage for nominating non-conflicted access requests for issuance to said memory cache structure; and

another stage for issuing to said cache memory structure at least one nominated request.

9. (Original) The circuit of claim 1 wherein said bank conflict comprises a bank conflict between at least one of said pending access requests and an older access request.

10. (Original) The circuit of claim 1 further comprising:

pending request queue to which said pending access requests for said cache memory structure are stored, wherein said bank conflict comprises a bank conflict between sibling access requests that are inserted to said pending request queue in parallel and wherein said bank conflict between sibling access requests is determined upon entry of said sibling access requests into said pending request queue.

11-20. (Canceled)

21. (Previously Presented) The circuit of claim 1 wherein said circuitry operable to determine said bank conflict is operable to determine said bank conflict before fully translating said virtual addresses to physical addresses.

22. (Canceled)

23. (Canceled)